ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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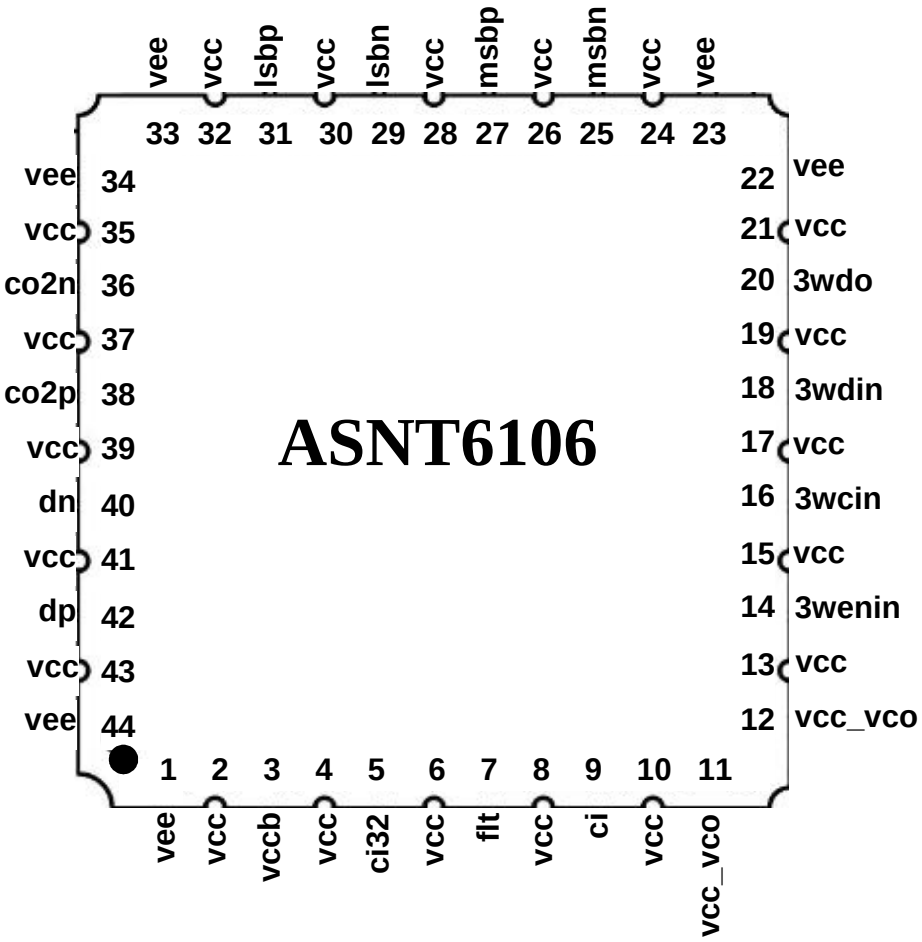
ASNT6106-KHS
60*Gbps*-30*Gbaud* PAM4 Decoder

- Converts one high-speed input PAM4 signal into two NRZ binary output signals
- On-chip clock recovery circuit
- Half-rate clock output synchronized with two output data signals
- Optional external full-rate clock input
- Fully differential CML input and output data, and output clock interfaces
- Single-ended CML compliant interfaces for input full-rate clock and input reference clock
- 1.2*V* CMOS 3-wire interface for digital controls
- Single -3.3*V* or +3.3*V* power supply
- Optional matching independent power supply for the clock recovery circuit
- Optional common mode adjustment in case of independent power supply for data input buffer
- Power consumption: under 2.4*W*
- Standard CQFN 44-pin package



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DESCRIPTION

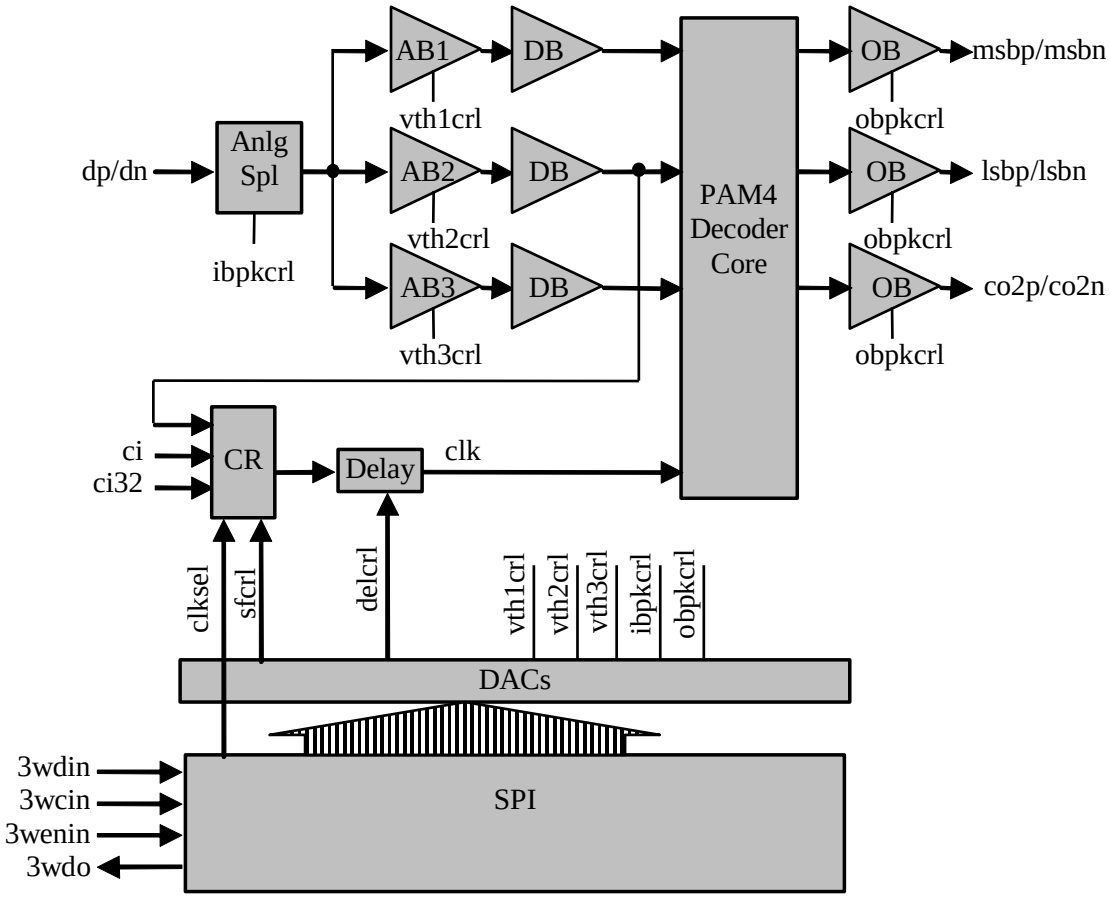

Fig. 1. Functional Block Diagram

PAM4 decoder with a built-in clock recovery circuit. A high-speed differential PAM4 input data signal dp/dn is processed by an analog splitter (Anlg Spl) with peaking adjustment capability. The three versions of the input signal are delivered to three analog buffers (AB1, AB2, and AB3) with adjustable differential thresholds. The resulting signals are converted into binary pulses by the three limiting digital buffers (DBs) and sent to a PAM4 Decoder Core. The output of the second DB is also sent to the clock recovery block (CR) that requires a low-speed reference clock applied to the port ci32 for correct operation. The part can also operate without clock recovery with an external high-speed clock applied to the port ci.

The three differential binary data streams in PAM4 Decoder Core are first retimed using a full-rate clock provided by the CR, and then decoded into two NRZ data signals. The phase of the retiming clock can be adjusted in respect to the data streams by an adjustable delay line (Delay).

The decoded most-significant and least-significant NRZ signals are retimed again, and delivered to the corresponding output ports msbp/msbn and lsbp/lsbn through Output Buffers (OBs). The retiming clock signal is divided by 2, and delivered to the output port co2p/co2n through a matching OB to ensure phase matching between the output data and clock signals.

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To reduce the physical number of pins, a 3-wire control interface (SPI) has been included in the chip. The SPI block provides all digital controls for the chip, and also controls digital-to-analog converters (DACs) that handle internal analog DC voltage adjustments.

Anlg Spl

The input Analog Splitter block accepts a PAM4 data signal at its differential CML-compatible input port dp/dn with on-chip single-ended 50*Ohms* terminations to vcc. The block has an adjustable frequency response controlled through SPI by the ibpkcrl signal as shown in Fig. 2. It should be noted that the higher control codes result in a certain increase of the block's currents.

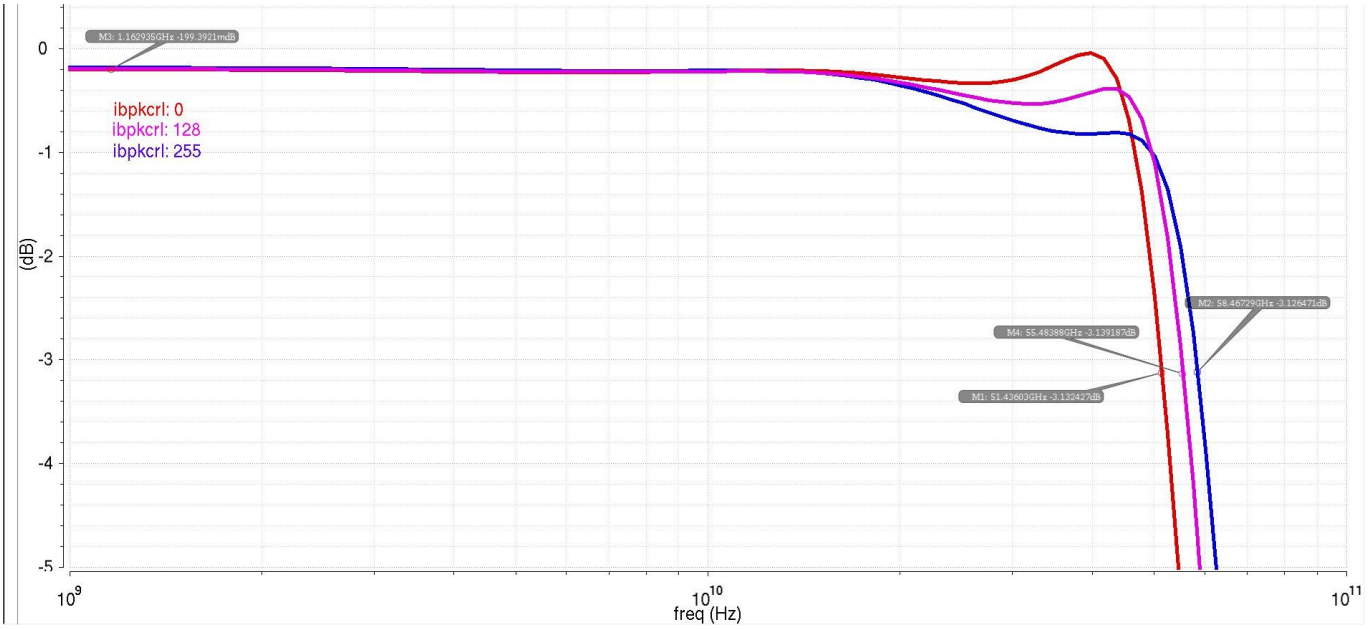

Fig. 2. Emitter Follower Currents of Anlg Spl Vs. Control ibpkcrl

ABs and DBs

Each Analog buffer (AB) accepts a copy of the input differential PAM4 signal with four logic voltage levels 00, 01, 10, and 11. The buffers can adjust the common mode voltages of their direct and inverted output signals using digital control signals vth1crl, vth2crl, and vth3crl provided by SPI. More specifically, vth1crl is used to shift the transition between the 10 and 11 levels to the differential output 0-crossing of AB1, and vth3crl is used to shift the transition between the 00 and 01 levels to the differential output 0-crossing of AB3. The control vth2crl can be used for fine tuning of the transition between the 01 and 10 levels and should usually be kept at its default value of 128. For an undistorted input signal, vth1crl and vth3crl should have the same value that is dependent on the input voltage swing. The maximum voltage shift in all ABs is additionally controlled by the cmicrl signal from the SPI where higher code values correspond to a large shift range.

For the correct operation of ABs at higher input voltage swings, their positive power supply vccb can be separated from vcc and biased by a higher voltage.

Fig. 3, Fig. 4, and Fig. 5 present the simulated dependence of differential output common mode voltages of ABs on the corresponding control signals.

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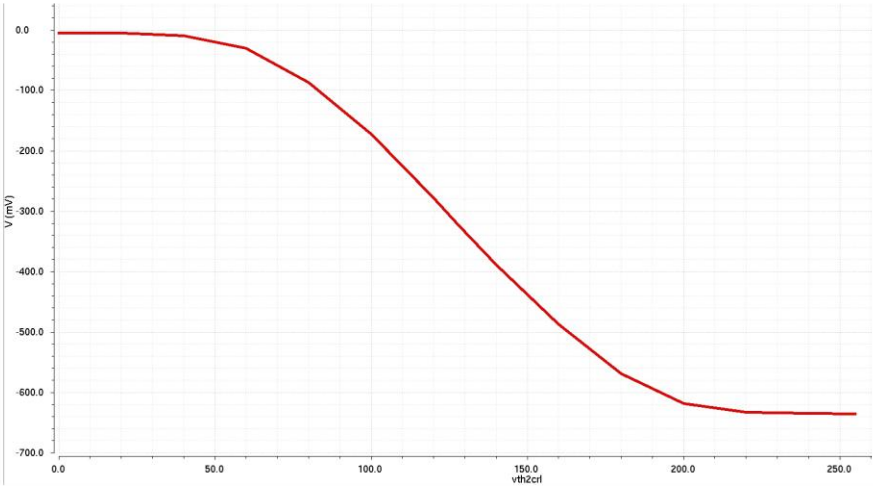

Fig. 3. Differential Common Mode Shift of AB1 vs. vth1crl

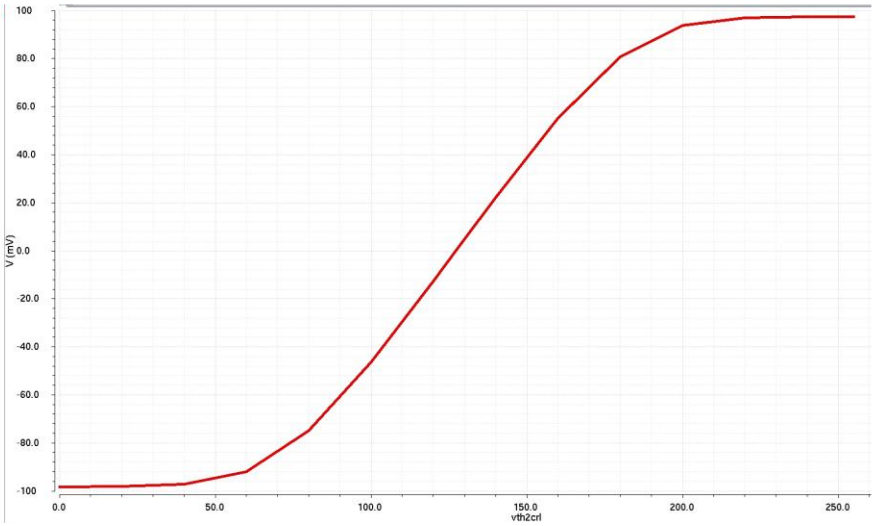

Fig. 4. Differential Common Mode Shift of AB2 vs. vth2crl

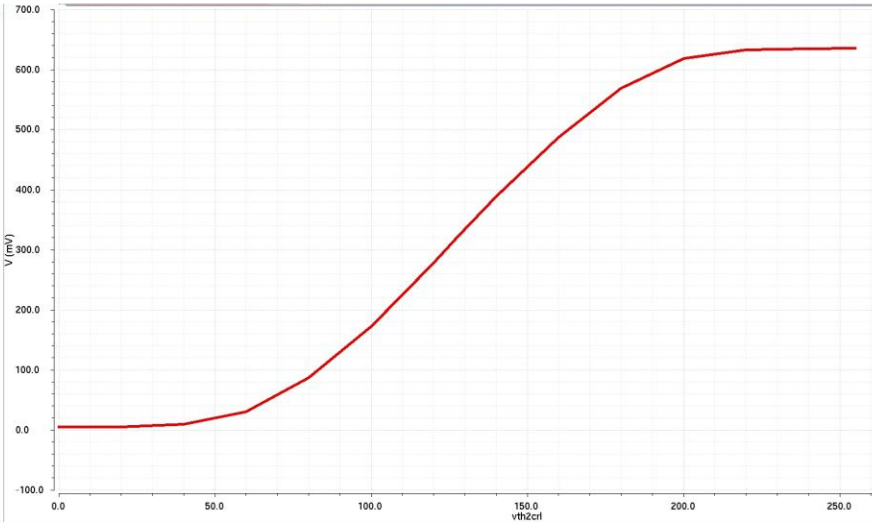

Fig. 5. Differential Common Mode Shift of AB3 vs. vth3crl

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One more SPI control signal buficrl can be used to adjust the currents of all ABs as shown in Fig. 6. The higher currents can be used to improve the linearity, and bandwidth of ABs, while the lower currents allow for power reduction.

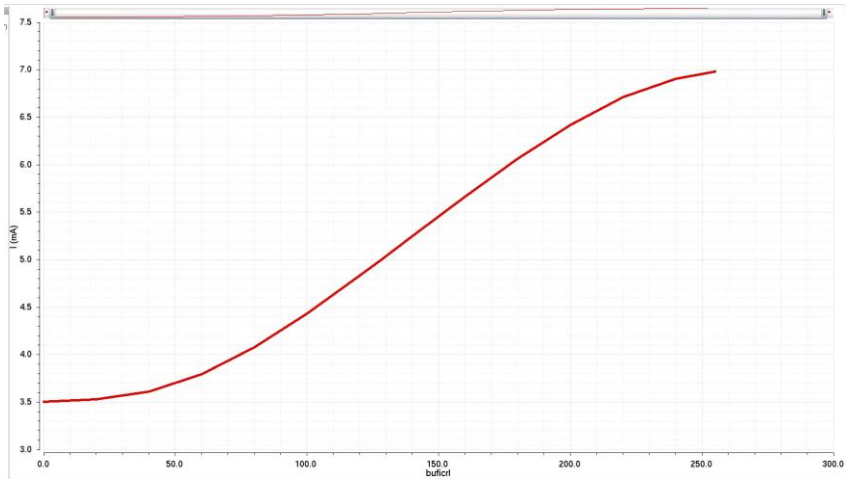

Fig. 6. DC Current of an AB Vs. buficrl

The resulting three analog signals of ABs are processed by three limiting digital buffers (DBs). The outputs of DBs are three binary differential signals. Transitions between the two logic voltage levels of these signals represent transitions in the top, middle, and bottom eyes of the input PAM4 signal.

PAM4 Decoder Core and OBs

The three digital binary differential signals from DBs are retimed in the Core by the full-rate clock which is provided by the CR block, and shifted by the Delay block. After this, the signals go through a decoder logic to form two differential digital binary data signals. The signals are retimed by the shifted full-rate clock, and sent to the output buffers. The full-rate clock goes through the clock dvider-by-2, and is sent to the identical output buffer. The edges of the data, and clock signals are exactly aligned at the outputs.

Three identical Output Buffers (OBs) with peaking control are used to deliver aligned data, and clock to the output pins. The influence of the control signal obpkcrl provided by the SPI is illustrated in Fig. 7.

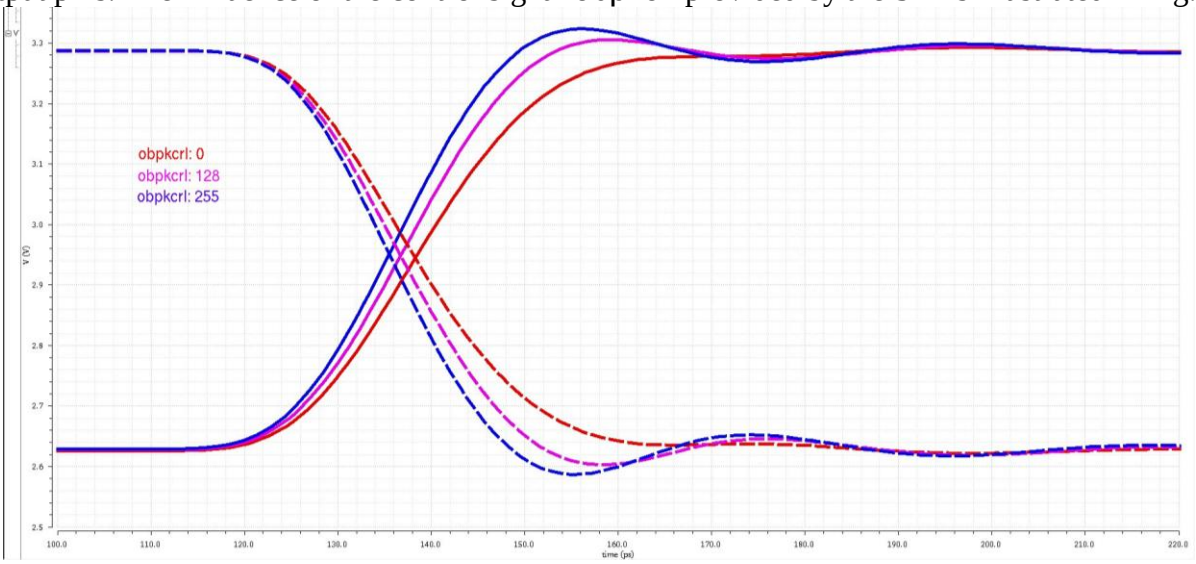

Fig. 7. OB Peaking Control

The output clock signal buffer can be switched off by the SPI control bit clokoff ="1".

CR

The CR block covers a wide range of input data rates (f_{bit}) by utilizing its three on-chip VCOs (voltage-controlled oscillators). The main function of the CR is to frequency-lock the selected on-chip VCO to the input data signal (clock recovery). The CR core contains a phase acquisition loop, and a frequency acquisition loop. The phase acquisition loop includes a high-speed Alexander Phase Detector (APD) that processes the input data stream dp/dn, and a clock signal generated by VCO. The frequency acquisition loop consists of a clock divider-by-16, and a PFD Potback block. The frequency loop works in concert with low-speed clock ci32. Both acquisition loops generate signals that control a single charge pump. The charge pump, in combination with a filter, generates an analog signal that controls the active VCO. The on-chip filter is small, so the CR requires a single off-chip filter shown in Fig. 8 to be connected to pin flt.

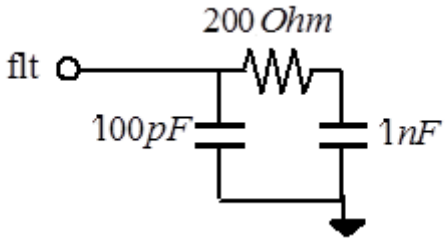

Fig. 8. External Loop Filter

By utilizing digital controls vcos0 and vcos1, the desired working frequency of the CR can be selected in accordance with Table 1 below.

Table 1. CR Mode Selection

vcos1	vcos0	VCO Operation Frequency (*GHz*)
"0" (0*V*)	"0" (0*V*)	External Clock
"0" (0*V*)	"1" (2.5*V*)	f_{min}≤18.8, f_{max}≥25.6
"1" (2.5*V*)	"0" (0*V*)	f_{min}≤22.5, f_{max}≥29.2
"1" (2.5*V*)	"1" (2.5*V*)	f_{min}≤28.6, f_{max}≥31.6

The loop gain can be adjusted by two digital controls icph, and icpl that control the charge pump current as shown in Table 2.

Table 2. Charge Pump Current Control

icph	icpl	Charge Pump current, *mA*
"0" (0*V*)	"0" (0*V*)	*I*max
"0" (0*V*)	"1" (2.5*V*)	*I*max-0.04
"1" (2.5*V*)	"0" (0*V*)	*I*max-0.27
"1" (2.5*V*)	"1" (2.5*V*)	*I*max-0.31

By utilizing the control byte sfcrl, the DC current of the control emitter follower of the active VCO can be adjusted linearly. Higher values of the control result in higher emitter follower currents. Higher emitter follower currents result in a more linear VCO frequency dependence on the control voltage at the expense of the frequency range.

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The control sfcrl can be used to adjust VCO frequency ranges by adjusting the VCO control voltage. Fig. 9 presents the dependence of the VCO control voltage shift on the control sfcrl.

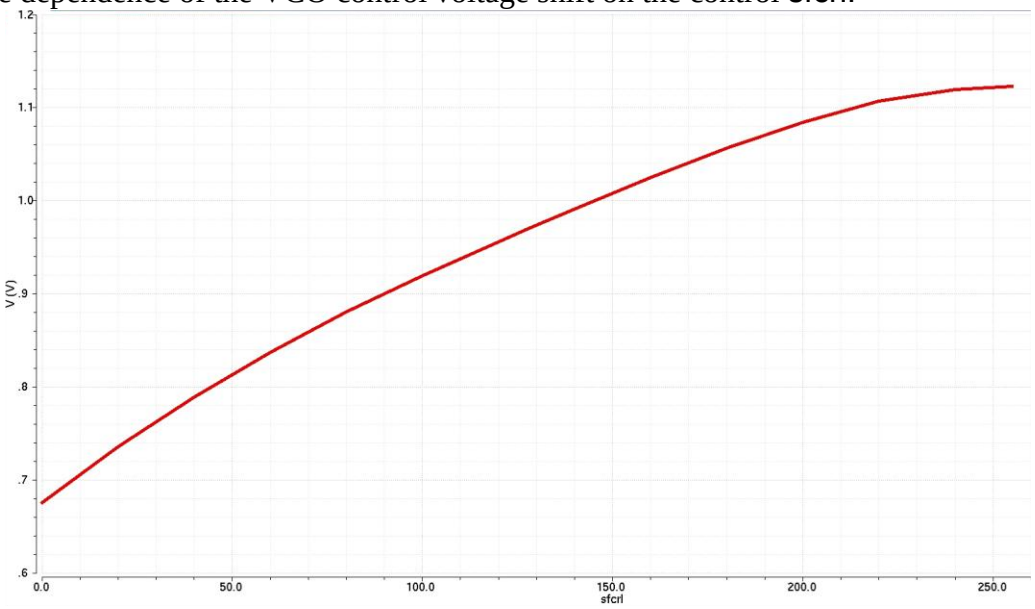

Fig. 9. VCO Control Voltage Shift Vs. Control sfcrl

The VCOs have a separate power supply from the rest of the chip in order to minimize noise. The VCO power is provided through pin vcc_vco.

In order to use an external clock, a full rate clock signal should be applied to the high-speed input clock pin ci in AC-coupling mode, and the pin ci32 does not have to be connected since the VCOs are not active.

Delay

The Delay block is used for selection of the optimal sampling point for the PAM4 input data signal. By utilizing the digital control byte delcrl, the phase of the recovered clock can be shifted with respect to the data as shown in Fig. 10.

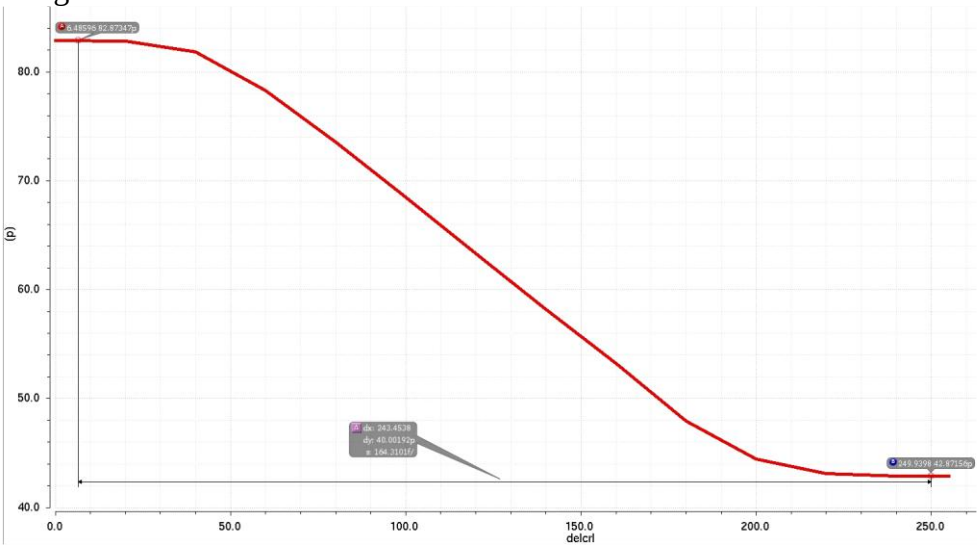

Fig. 10. Latency of the Delay Block Vs. delcrl

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3-Wire Interface Control Block

To reduce the physical number of control inputs to the chip, a 10-byte shift register with a 3-wire input interface has been included on chip. The SPI block is powered by an internally generated supply voltage of +1.2*V* from vee. The digital control bits applied through 3wdin input are latched in, and shifted down the register with the clock 3wcin. The write enable signal 3wenin must be set to logic "0" during the data read-in phase. The SPI data can be monitored through the output 3wdo. Table 3 presents the byte order of the 3-wire interface block.

Table 3. Control Bytes

Byte #	Bit #	Bit order	Signal name	Signal function
1	From 7	MSB	cmicrl	Vth control range
	to 0	LSB		
2	From 7	MSB	vth1crl(8:1)	MSB bits of Vth1 control
	to 0	LSB		
3	From 7	MSB	vth2crl	Vth2 control
	to 0	LSB		
4	From 7	MSB	vth3crl(8:1)	MSB bits of Vth3 control
	to 0	LSB		
5	From 7	MSB	buficrl	AB current control
	to 0	LSB		
6	From 7	MSB	delcrl	Clock delay control
	to 0	LSB		
7	From 7	MSB	sfcrl	VCO frequency range control
	to 0	LSB		
8	From 7	MSB	ibpkcrl	Analog Buffer peaking control
	to 0	LSB		
9	From 7	MSB	obpkcrl	Output peaking control
	to 0	LSB		
10	7		vth1crl(0)	LSB bit of Vth1 control
	6		vth3crl(0)	LSB bit of Vth3 control
	5		icph	Charge pump current adjustment, see Table 2
	4		icpl	
	3		vcos1	CR mode selection, see Table 1
	2		vcos0	
	1		clkoff	Clock OB OFF/ON
	0		-	Constant "0"

The SPI load order is illustrated in Fig. 11.

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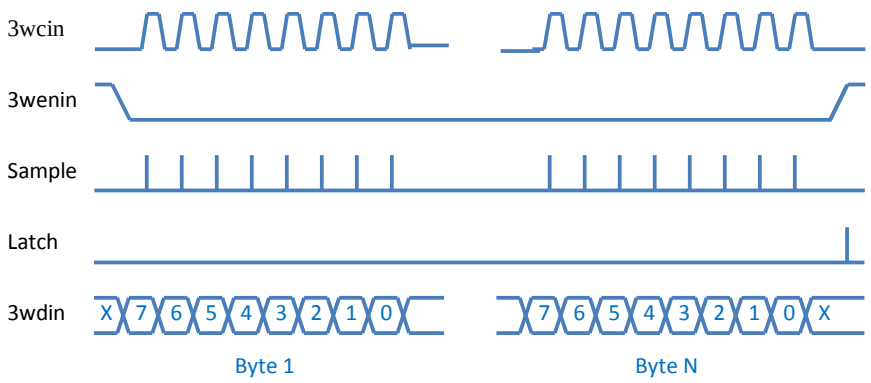

Fig. 11. SPI Load Order

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* = ground and vee = -3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 3.3*V* and vee = 0*V* (external ground)

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 4 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.8	*V*
Power Consumption		2.4	*W*
Input Voltage Swing (SE)		1.0	*V*
Case Temperature*)		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dp	42	Input	CML differential data inputs with internal SE 50*Ohms* termination to VCC
dn	40		
ci	9	Input	SE full-rate clock input with internal 50*Ohms* termination to VCC_VCO
msbp	27	Output	CML differential data outputs. Require external SE 50*Ohms* termination to VCC
msbn	25		
lsbp	31	Output	CML differential data outputs. Require external SE 50*Ohms* termination to VCC
lsbn	29		
co2p	38	Output	CML differential half-rate clock outputs. Require external SE 50*Ohms* termination to VCC
co2n	36		
Low-Speed I/Os			
ci32	5	Input	SE clock input with internal 50*Ohms* termination to VCC
3wenin	14	1.2*V* CMOS input	Enable input signal for 3-wire interface
3wcin	16		Clock input signal for 3-wire interface
3wdin	18		Data input signal for 3-wire interface
3wdo	20	1.2*V* CMOS output	Data output signal of 3-wire interface
Controls			
flt	7	I/O	External CR filter connection

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Main positive power supply (+3.3*V*)	2, 4, 6, 8, 10, 13, 15, 17, 19, 21, 24, 26, 28, 30, 32, 35, 37, 39, 41, 43
vccb	Positive power supply for input buffers (VCC to VCC+0.6V)	3
vcc_vco	Positive power supply for VCO (VCC)	11, 12
vee	Negative power supply (GND or 0*V*)	1, 22, 23, 33, 34, 44

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.0	+3.3	+3.6	*V*	±9%
vcc_vco		vcc		*V*	
vccb	+3.0	+3.3	+3.9	*V*	Depends on input swing
vee		0.0		*V*	
I_{vee}	640		730	*mA*	Depends on settings
Power Consumption	2.2		2.4	*W*	
Junction Temperature	-25	50	125	*°C*	
HS Input Data (dp/dn)					
Data Rate			30	*Gbaud*	PAM4
Swing p-p (Diff or SE)	0.05		1.0	*V*	With increased vccb
CM Voltage Level	vcc-0.8		vcc	*V*	
HS Input Clock (ci)					
Frequency			30	*GHz*	
Swing p-p (Diff or SE)	0.05		0.8		
CM Voltage Level	vcc-0.8		vcc		
LS Input Reference Clock (ci32p)					
Frequency	585.9375		987.5	*MHz*	
Swing p-p (Diff or SE)	0.06		0.8	*V*	
CM Voltage Level	vee		vcc	*V*	
Duty Cycle	40	50	60	*%*	
HS Output Data (msbp/msbn, lsbp/lsbn)					
Data Rate			30	*Gbps*	30*Gbaud* input
Logic “1” level		vcc		*V*	
Logic “0” level	vcc -0.66		vcc -0.6	*V*	
Delay from ci		Clock period + 115		*ps*	Falling edge, no CR mode
Delay from co2				*ps*	Falling edge, CR mode
Jitter		2	4	*ps*	peak-peak
HS Output Half-Rate Clock (co2p/co2n)					
Clock Rate	11.8		16	*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level	vcc -0.66		vcc -0.6	*V*	
Jitter		2	4	*ps*	peak-peak
3-Wire Inputs (3wdin, 3wcin, 3wenin)					
High voltage level	vee+1.1		vee+1.35	*V*	
Low voltage level	vee		vee+0.35	*V*	
Clock speed		350	400	*MHz*	

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PACKAGE INFORMATION

The chip die is housed in a custom, 44-pin CQFN package shown in Fig. 12. The package provides a center heat slug located on the back side of the package to be used for heat dissipation. ADSANTEC recommends using extreme caution when soldering this section to the board to avoid overheating. It should be connected to the VCC plain that is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6106-KHS. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

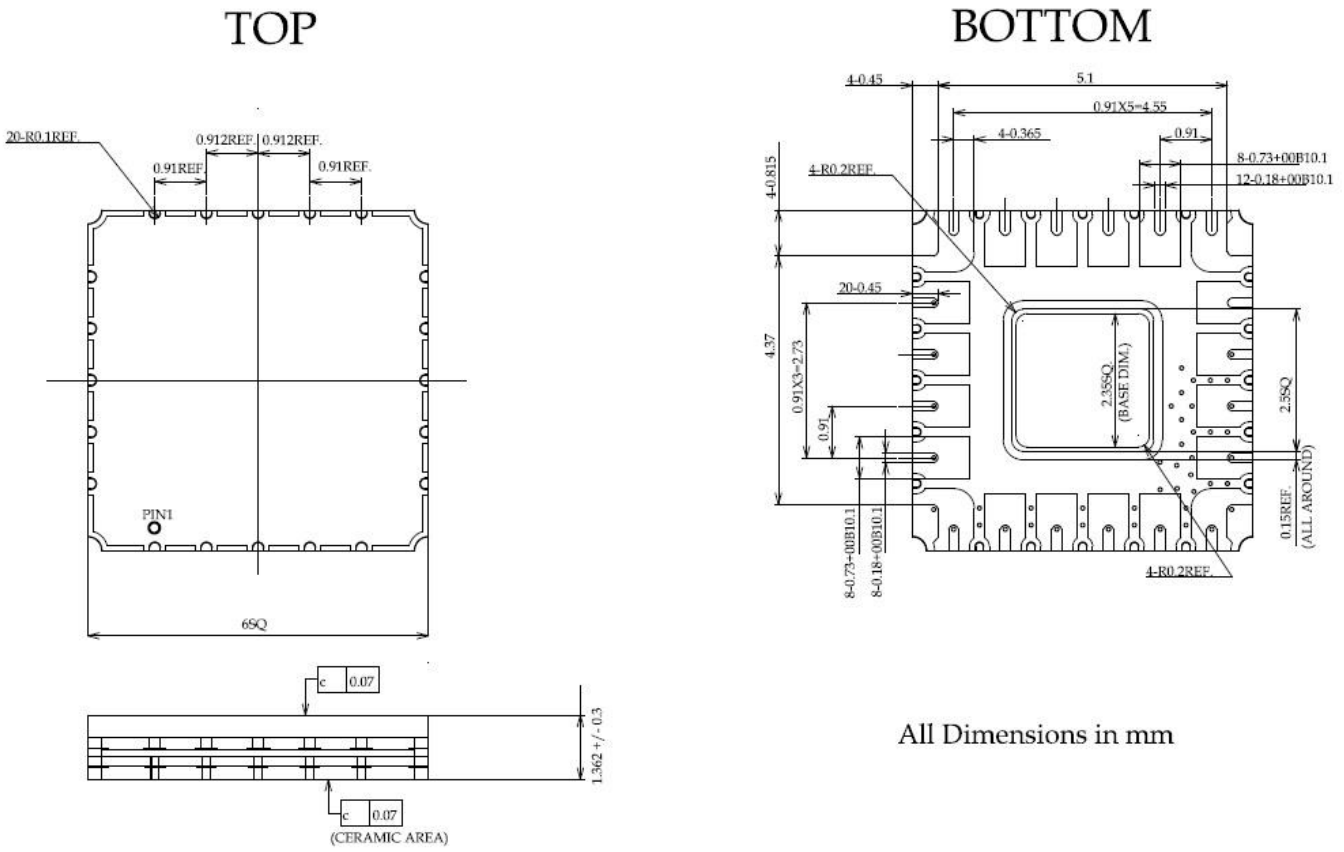

Fig. 12. CQFN44 Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.2.2	04-2023	Updated Loop Filter Information Updated VCO Frequency Ranges Updated Reference Clock Range
1.1.2	04-2023	Updated Package Drawing
1.0.2	04-2023	First release Corrected maximum data rate
0.2.2	04-2023	Updated Package Drawing
0.1.2	12-2022	Corrected terminal function numbers to match pin-out diagram
0.0.1	03-2022	Preliminary release