

EOLQ-8540G-PCT-XX Series

Multi-Mode 40GBASE-SR4 QSFP+ Transceiver RoHS Compliant

Features

- ◆ Compliant to the IEEE 802.3ba(40GBASE-SR4)
- ◆ 40Gbps aggregated bidirectional data throughput
- Compliant to the QSFP+ MSA SFF-8436
 Specification
- ◆ Active Optical Cables Length up to 100m
- VCSEL array transmitter and PIN array receiver
- ◆ Low Power dissipation <0.35W per channel
- Infiniband 4XQDR/40G Base-SR10 Compliant Laser Class 1
- ◆ Operating Case Temperature: 0°C~+70°C
- ◆ Safety Certification: TUV/UL/FDA*Note*
- ◆ RoHS Compliant



Applications

- InfiniBand QDR (4 x 10G), DDR (4 x 5G) and SDR (4 x2.5G) interconnects
- High Performance and High Productivity computer interconnects
- Data Aggregation, Backplane and Proprietary Density Applications
- PCI-Express, SAS/SATA, Fibre Channel compatible interconnect
- Datacom and Telecom switch and router backplane connections

Ordering Information

Part No.	Data Rate	AOC Length*(note2)	Temp.	DDMI
EOLQ-8540G-PCT-XX*(note1)	40Gbps	1~100m	0℃~+70℃	Yes

Note1: Standard version.

Note2: Length measured OM3 fiber. XX denotes the AOC length with unit meter. For example, 01 denotes 1m, 02 denote 2m ... 99 denote 99m and 1H denotes 100m.

Note*: For the latest certification information, please check with Eoptolink.

^{*}The product image only for reference purpose.



Absolute Maximum Ratings*

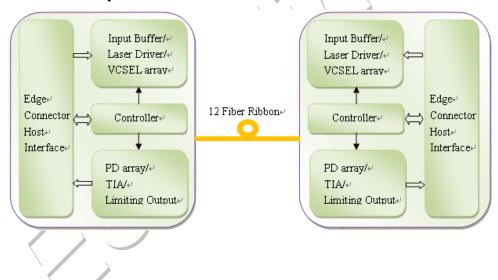
Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%

^{*}Exceeding any one of these values may destroy the device immediately.

Recommended Operating Conditions

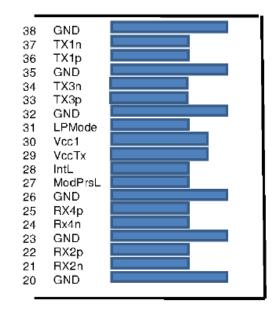
Parameter	Symbol		Min.	Typical	Max.	Unit
Operating Case Temperature	T _c	EOLQ-8540G-PCT-XX	0		+70	°C
Power Supply Voltage	Vcc		3.15	3.3	3.45	V
Aggregate Bit Rate	BR _{AVE}			41.25		Gbps
Lane Bit Rate	BR _{LANE}			10.3125		Gbps

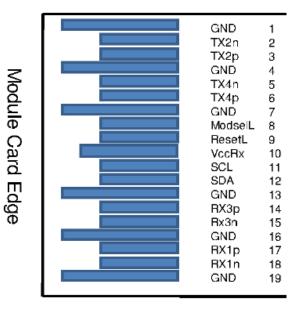
Functional Description of Transceiver





QSFP+ Transceiver Electrical Pad Layout





Top Side Viewed From Top

Bottom Side Viewed From Bottom

Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1



QSFP+ Series

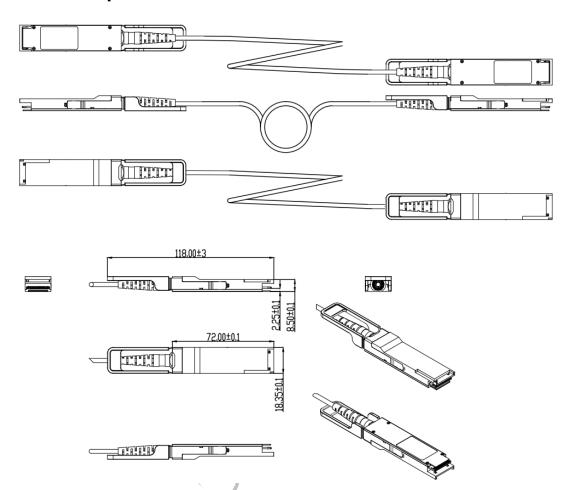
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Тх3р	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

^{1:} GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

^{2:} Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500mA.



Mechanical Specifications



*This 2D drawing only for reference, please check with Eoptolink before ordering

Obtaining Document

You can visit our website: http://www.eoptolink.com

Or contact Eoptolink Technology Inc., Ltd. listed at the end of the documentation to get the latest documents.

Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Kelly			Preliminary.	July 2, 2012
V1.b	Kelly			Add photo.	Oct 30, 2012
V1.c	Angela	Kelly		Released	Feb 21,2014
				Update Mechanical	
	Marvin	Angela		Specification, picture,	
V1.d				regulatory	Jan 27,2018
				compliance and	
				contact.	
	Nico	Nico Marvin/Peter/		Update the product	
V1.e				image, the regulatory	Aug 29, 2018
		Chao		compliance and the	



QSFP+ Series

			2D drawing.	
			Delete the regulatory	
V1.f	Elaine	Kelly/Yiwei.Chen	compliance, updated	Dec 18, 2018
			the features.	

Notice:

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