DC to 44GHz / 12dB Gain/ 21dBm P_{SAT} Medium Power amplifier

DATA SHEET **VWA 5000054 AA**

General Description

The **VWA5000054AA** is a distributed amplifier designed on a 0.15µm pHEMT process.

The device includes an internal biasing circuit which can be used to feed directly the drain current, as an alternative to bias the drain from the RF Output access. Depending on the desired low cut off frequency, external components can be added to ensure operations started from 30KHz to 2GHz through up to 40GHz. The device includes also an embedded output signal detector and an embedded input gate biasing circuit which can be used to reduce the power consumption in many linear receiving amplifier chains. It is capable of more than +21dBm of output power at saturation regime, up to 40GHz. And more than +17dBm of output power at 1dB of gain compression, up to 34GHz. It provides more than 12dB of linear gain from DC to 44GHz with a positive slope of +0.0375dB/GHz, up to 40GHz. This device can provide up to 10dB gain up to 50GHz with an excellent group delay. Optimized biasing configurations are proposed depending on the input power level pattern.

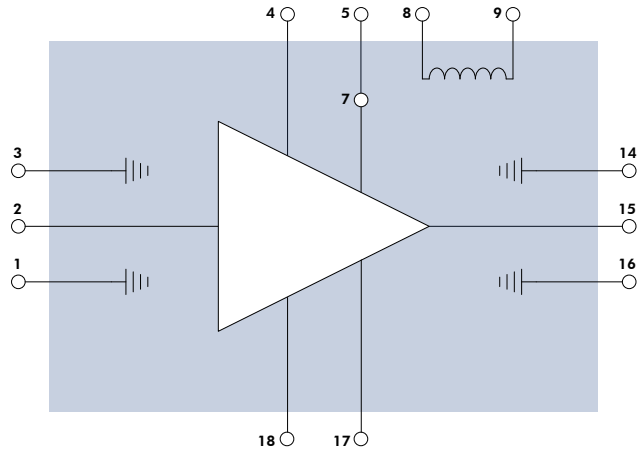
Features

- Wideband Distributed amplifier pHEMT GaAs MMIC
- Wide band: DC to 46GHz.
- Internal biasing access.
- Flat group delay.
- 50ΩRF Single ended input and output
- DC coupled In, DC coupled Out
- P_{1dB} >+17dBm DC to 34GHz
- High output P_{SAT}>+21dBm DC to 40GHz
- Small signal gain : >12dB from 2GHz to 40GHz
- Nominal Power Supply: 168mA @ +6V
- Chip size: 2.29 x 1.575 x 0.1mm

Applications

- Up to 50GBps, E/O Modulator driver (3V/75mA)
- Radar / ECM / ECCM
- Receiver chain amplification
- Wide band MPA
- Radar / ECM / ECCM
- Test and measurement
- Broadband / datalink communication

Pins Assignement & Functional Block Diagram



Symbol	Pad N°
RF In	2
V_{G2}	4
V_{D_LOAD}	5
$V_{DL\ In}$	7
V_{SELF} Out	8
V_{SELF} In	9
RF Out	15
V_{G1_A}	17
V_{G1_B}	18
GND	1/3/14/16

Electrical Specifications (Test Under Probes)

K Connector housing using Internal Biasing Circuit.

- Tamb.= +25°C
- V_D = +6V
- I_D = 162mA
- V_{G1_A} = 0V
- V_{G2} = +2.5V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	DC		40	Ghz
G	Small signal gain		12.5		dB
ΔG	Small signal gain flatness		+/-1		dB
S11	Input return loss		-10	-7	dB
S22	Output return loss		-12		dB
P1dB	Output P1dB	17	18		dBm
P_{SAT}	Saturated output power		21		dBm
I_D	Drain current		162		mA
V_D	Drain supply voltage		6		V

Environmental parameters

Symbol	Parameter	Values	Unit
Top	Operating temperature range	-40/+85	°C
Tstg	Storage temperature range	-55/+85	°C

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_D	Drain bias voltage		9	V
Pin	RF input power		18	dBm
Pcw	Continuous power disspation(@85°)		2.5	W
T process	Temperature process max 20 seconds		325	°C

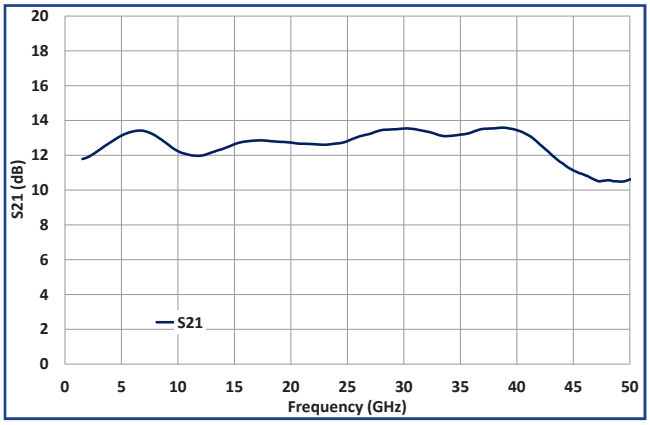
Operation of this device above any of these parameters may cause permanent damage.

Typical Performances (Test Under Probes)

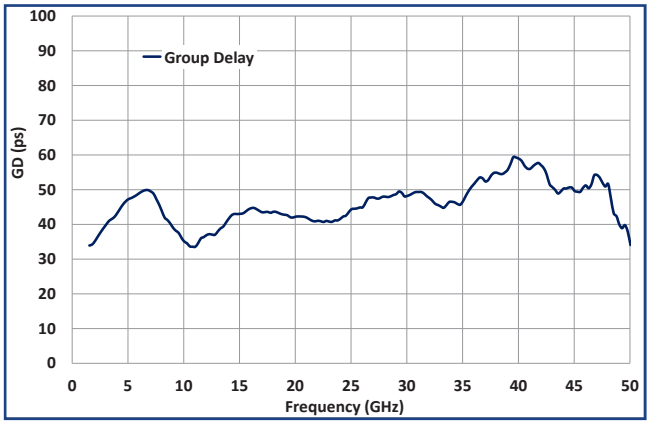
Test conditions unless otherwise noted:

- Tamb.= +25°C
- V_D = +6V
- I_D = 162mA
- V_{G1_B} = left open
- V_{G2} = +2.5V

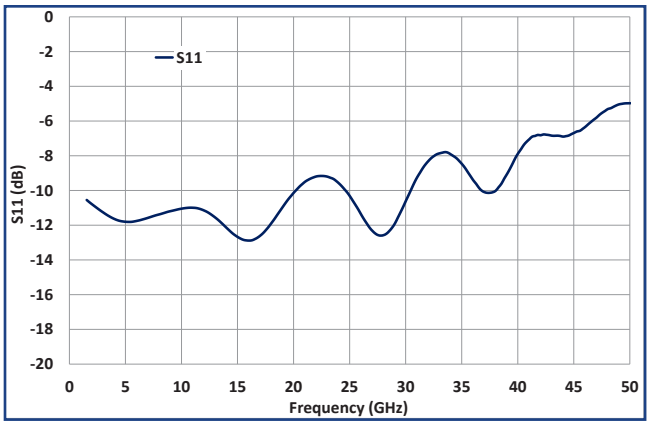
Small Signal Gain



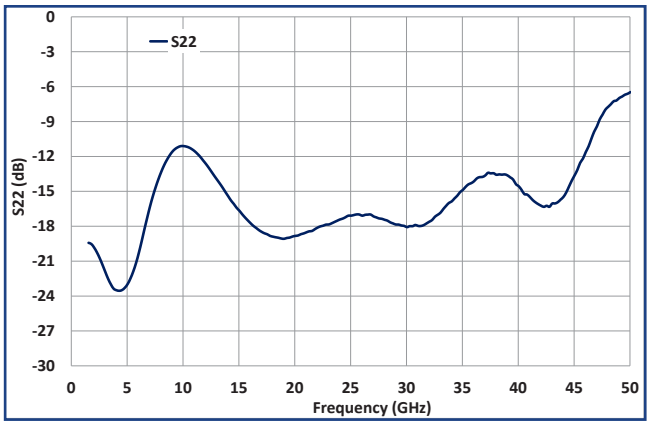
Group Delay



Input Return Loss



Output Return Loss



Typical Performances (K connector housing)

K Connector housing using Internal Biasing Circuit.

Blue curve

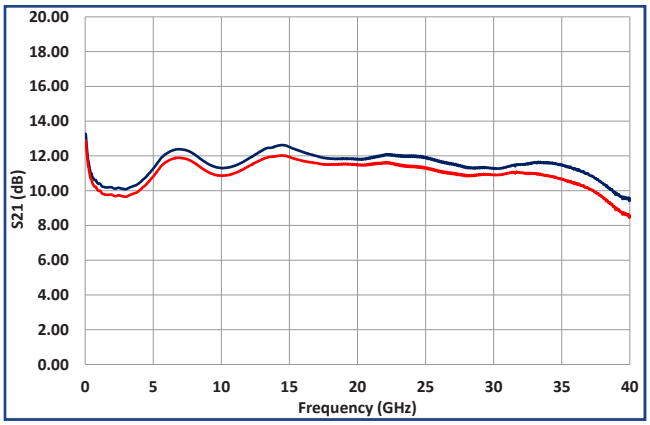
- Tamb.= +25°C
- V_D = +6V
- I_D = 162mA
- V_{G1_B} = left open
- V_{G2} = +2.5V

Red curve

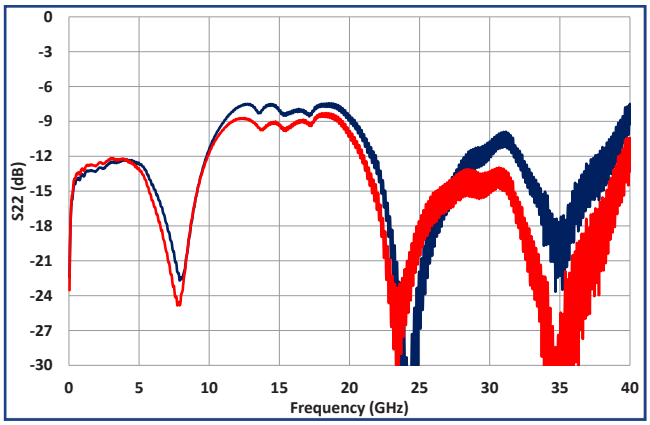
- Tamb.= +25°C
- V_D = +5V
- I_D = 70mA
- V_{G1_B} = -11V
- V_{G2} = +1.6V

Note : This configuration with external inductor help to ensure applications from 30KHz to up to 40GHz. For application from 2GHz to 40GHz, an external capacitor can be used instead of external inductors.

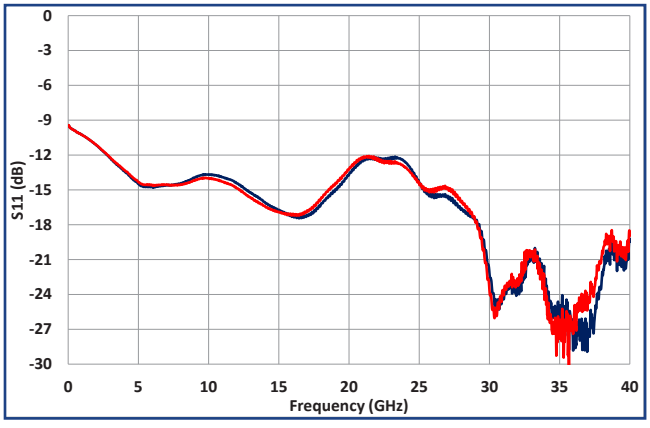
Small Signal Gain



Output Return Loss



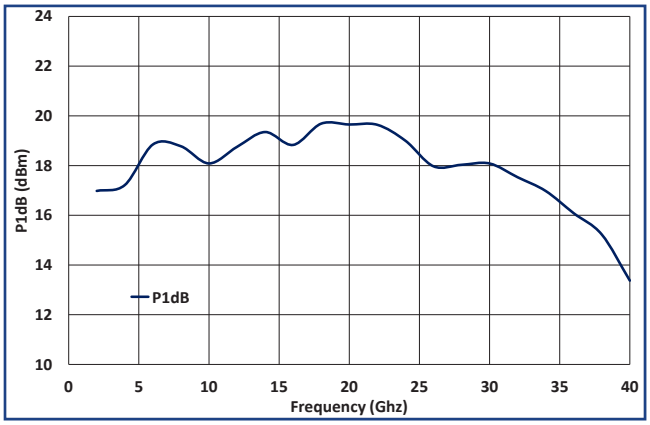
Input Return Loss



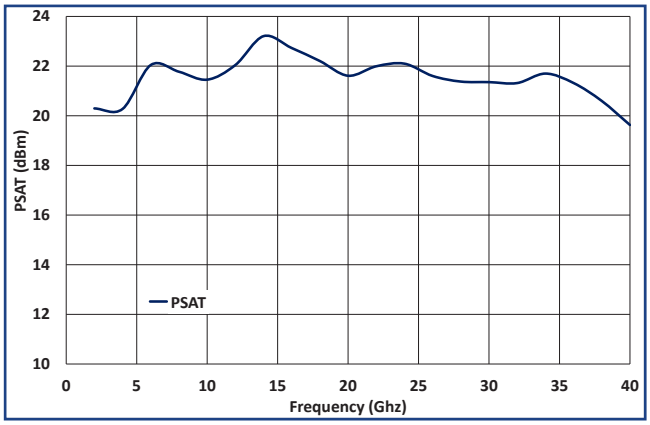
K Connector housing using Internal Biasing Circuit.

- Tamb.= +25°C
- V_D = +6V
- I_D = 162mA
- V_{G1_B} = left open
- V_{G2} = +2.5V

Output P1dB



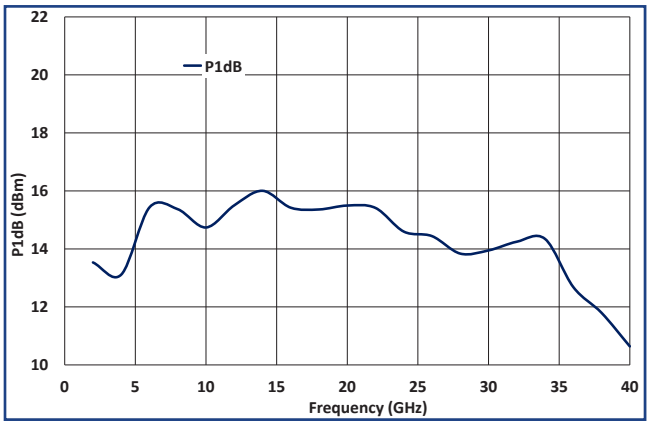
Saturated Output Power



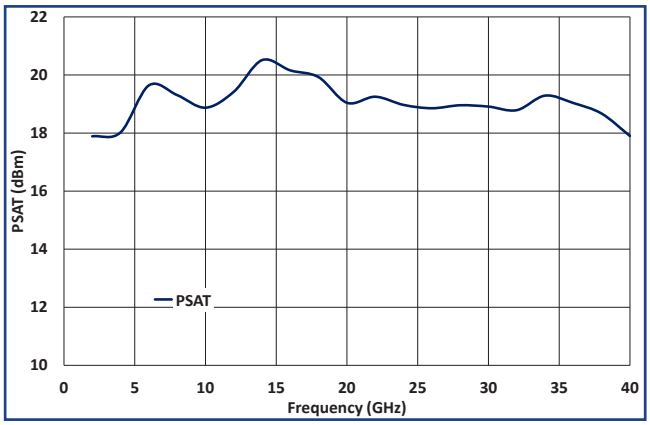
K Connector housing using Internal Biasing Circuit.

- Tamb.= +25°C
- V_D = +5V
- I_D = 70mA
- V_{G1_B} = -11V
- V_{G2} = +1.6V

Output P1dB



Saturated Output Power



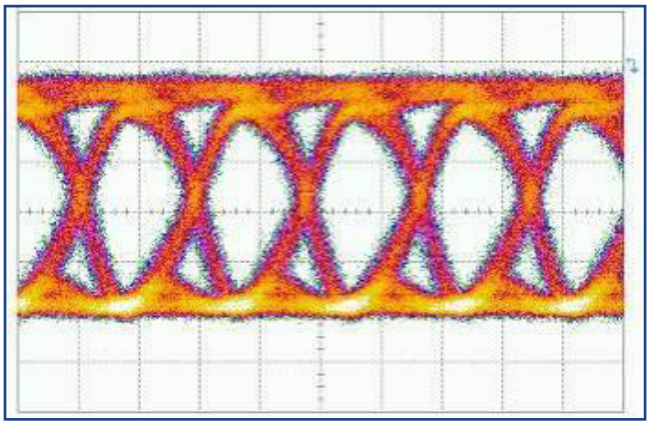
Telecoms Measurement (K connector housing)

K Connector housing using Internal Biasing Circuit.

- V_D = +5V
- I_D = 70mA
- V_{G1} = left open
- V_{G2} = +1V

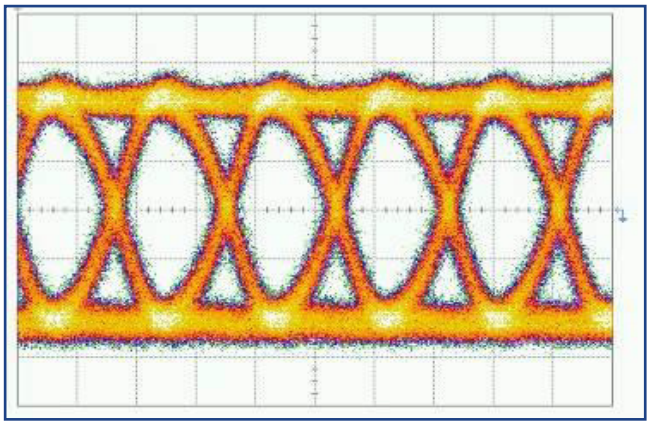
Measure on Agilent 86100C, without precision time base and with 50GHz electronic head.

28GBps Input Eye diagram



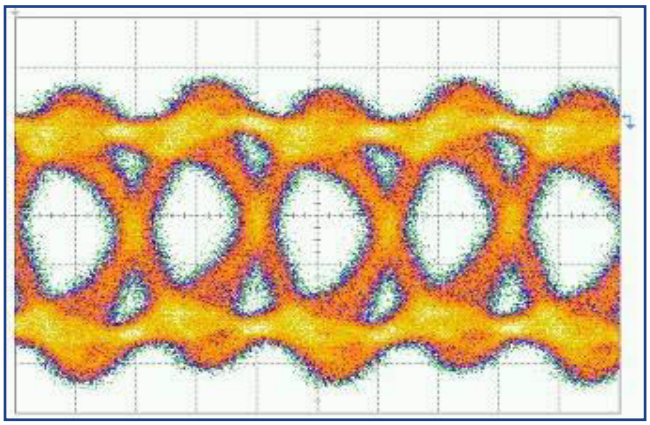
0.6Vpp Intput Eye diagram: Time scale 20ps/div, amplitude scale= 150mV/div.

28GBps Output Eye diagram



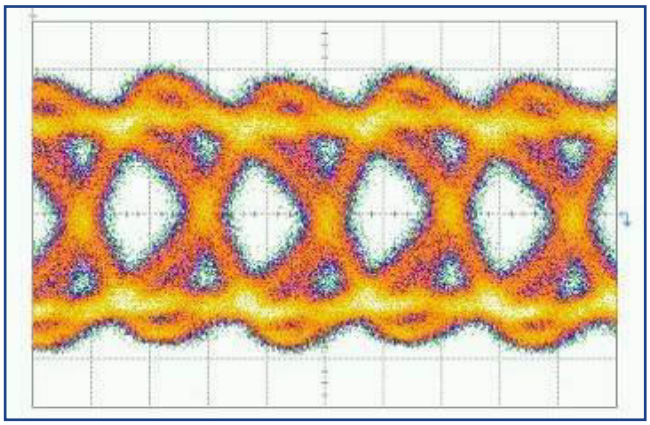
2.2Vpp Output Eye diagram: Time scale 20ps/div, amplitude scale= 400mV/div.

50GBps Input Eye diagram



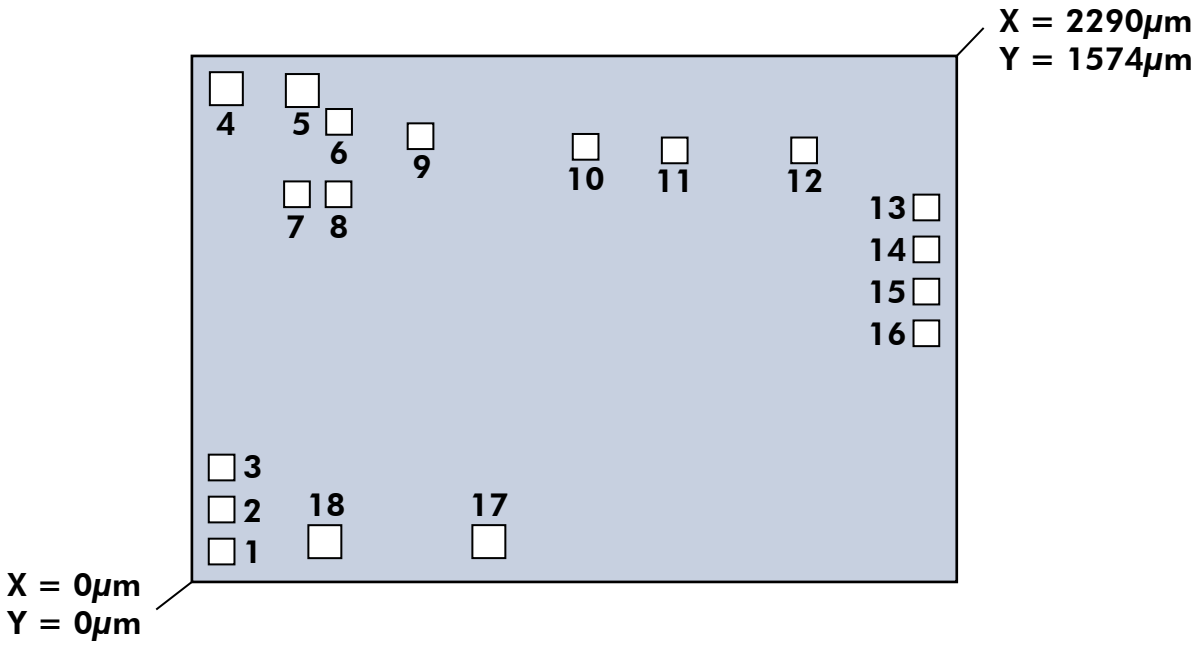
0.7Vpp Intput Eye diagram: Time scale 10ps/div, amplitude scale= 150mV/div.

50GBps Output Eye diagram



3Vpp Output Eye diagram: Time scale 10ps/div, amplitude scale= 500mV/div.

Die Layout



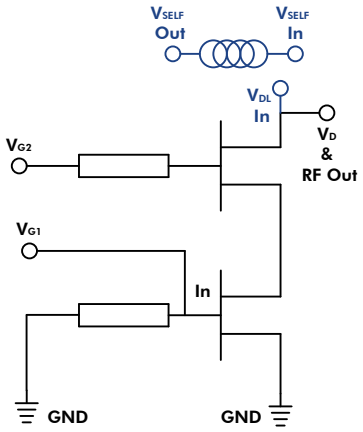
Pinout and Bonding Pad Coordinates

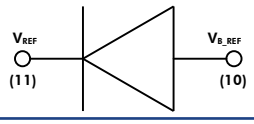
Die Pin Out				
Pad	**X (µm)**	**Y (µm)**	**Size (µm x µm)**	**Function**
1	90	92	75x75	GND
2	90	217	75x75	RF In
3	90	342	75x75	GND
4	102	1478	100x100	V_{G2}
5	330	1472	100x100	V_{D_LOAD}
6	441	1377	75x75	RA
7	315	1160	75x75	V_{DL}_In
8	440	1160	75x75	V_{SELF}_Out
9	685	1335	75x75	V_{SELF}_In
10	1180	1305	75x75	V_B_Ref
11	1446	1291	75x75	V_{REF}
12	1834	1291	75x75	V_{DET}_Out
13	2199	1121	75x75	V_{DET}_In
14	2199	996	75x75	GND
15	2199	871	75x75	RF Out
16	2199	746	75x75	GND
17	890	119	100x100	V_{G1_A}
18	400	119	100x100	V_{G1_B}

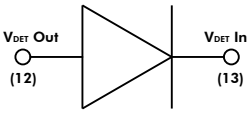
Die thickness = 100µm
Die bottom must be connected to ground (RF and DC)

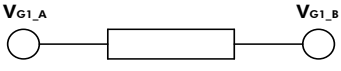
Access Description

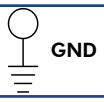
Pin Number	Name	Description	Electrical interface
2	RF In	RF input, This access is DC coupled and internally matched to 50Ω.	
4	V_{G2}	Gate control input access for second stage distributed amplifier structure. Apply +2.5V for nominal biasing conditions.	
5	V_{D_LOAD}	Drain termination load decoupling access. This access must be connected to a MIM 100pF or 1000pF capacitor, with a low	
15	RF Out	RF output, This access is DC coupled and internally matched to 50Ω. It can also be used to feed the drain current (ID), by using a wide bandwidth external Bias-T structure.	
7	V_{DL}_In	Input drain line access, if internal biasing circuit is used, it must be connected to VSELF_IN by using a small bonding wire connection.	
8	V_{SELF}_Out	Biasing circuit input pad access, if internal biasing circuit is used; it must be connected to VDD power supply. Depending on the working bandwidth, some additional external components can be added (See end of documents for explanations).	
9	V_{SELF}_In	Biasing circuit embedded pad access, if internal biasing circuit is used; it must be connected to VDL_IN by using a small bonding wire connection.	
10	V_{B_REF}	Biasing reference diode access	
11	V_{REF}	Reference diode voltage access	
12	V_{DET}_Out	Detector output	
13	V_{DET}_In	Detector Input	
17	V_{G1_A}	Gate control output access for first stage distributed amplifier structure. It can be connected to a negative power supply voltage source in order to decrease the drain current consumption. Or it can be left open.	
18	V_{G1_B}	Gate control input access for first stage distributed amplifier structure. It can be connected directly to the amplifier access by a small bonding wire.	
Die Bottom	GND	Die must be connected to HF and DC ground	







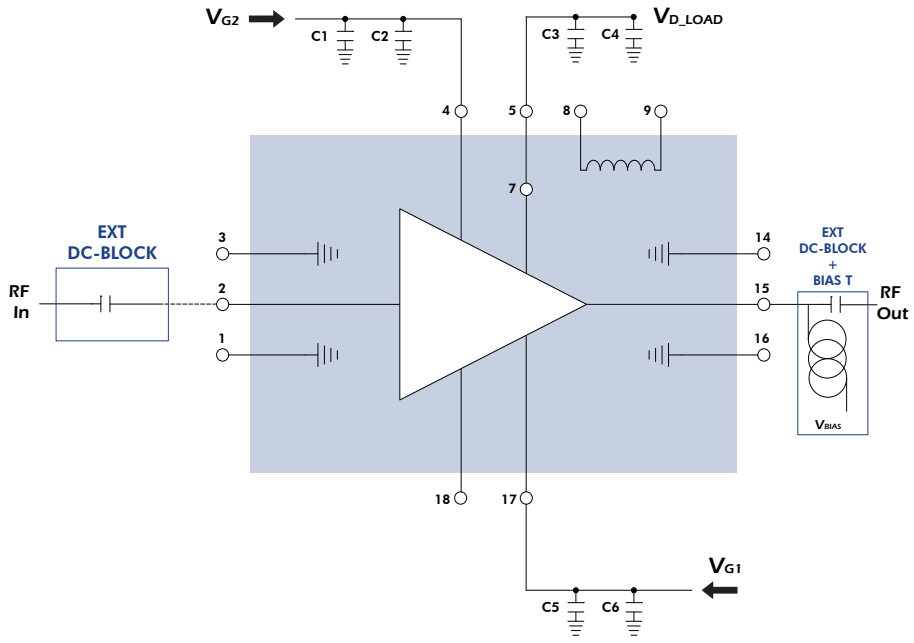




Application Circuit

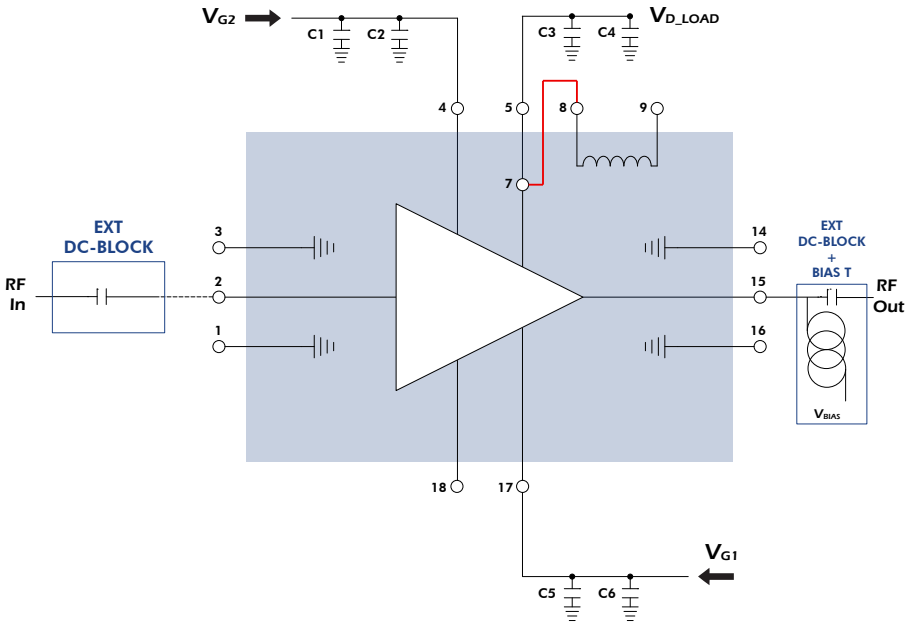
Configuration A

- C1, C4 and C6 = 1µF
- C2, C3 and C5 = 1nF capcitors are MIM type and must be placed as close as possible to the die access.



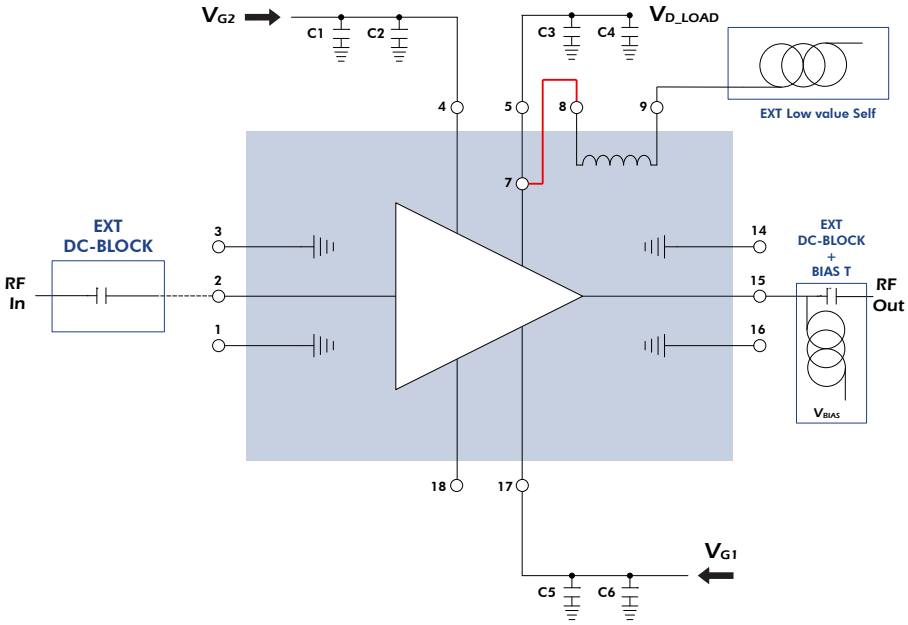
Configuration B

- C1, C4 and C6 = 1µF
- C2, C3 and C5 = 1nF capcitors are MIM type and must be placed as close as possible to the die access.



Configuration C

- C1, C4 and C6 = 1µF
- C2, C3 and C5 = 1nF capcitors are MIM type and must be placed as close as possible to the die access.



Ordering Information

Product Code	Definition
VWA 5000054AA	DC To 44GHz / 12dB Gain / 21dBm P_{SAT}

Associated Material

Material	Status
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
Packaged die Evaluation Board (packaged die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measurents files (S2P)	Contact factory

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3 - 4 minutes, maximum

ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave:

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Represented by

VectraWave

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