V5054

30-Port 1394b AS5643 PCI Express FPGA Card

Benefits

High density 1394b PCIe FPGA Card for SAE-AS5643 aerospace applications and test stands

Supports transformer-coupled S200/S400 data rates

A COTS solution optimized for SWaP (size, weight and power)

Programmable FPGA with a powerful development framework

Next generation host interface connection bandwidths

STOF & AS5643 offload for superior timing tolerance and test repeatability

Wide range of FPGA sizes and memory configuration options

Features

Thirty transformer-coupled ports (optionally non-transformer-coupled)

Physical ports are configurable for up to ten different 1394b nodes, with three ports in each node

Two Link Layer Controller Host Interface IP Core options:

- Open Host Controller Interface (OHCI) with STOF offload
- Direct DMA with AS5643 hardware offload

Xilinx Kintex UltraScale FPGA (KU115)

Supports PCIe Gen3 x 8

PPS time synchronization with nSec resolution

Thermal sensors for monitoring card temperature

Robust FPGA development framework

Linux and Windows drivers available

Overview

The V5054 is the highest density 1394b PCIe card available on the market. The V5054 has been designed specifically for 1394b AS5643 aerospace application development and test stand purposes.

The V5054 provides thirty front panel transformer-coupled 1394b ports (non transformer-coupled ports option available). The host interface provided is Gen3 x 8 PCIe.

The V5054 supports industry standard 1394 Open Host Controller Interfaces (OHCI), OHCI with STOF offload, and AS5643 offload Link Layer Controller IP Cores

- An industry standard OHCI interface with hardware-based offload of the AS5643 STOF.
- An AS5643 hardware offload engine providing complete packet formation, ASM label checking, and direct DMA with the host.

For more information on the New Wave DV 1394 FPGA IP cores visit: https://newwavedv.com/products/ip-cores/1394b-as5643/.

The thirty front panel ports are perfect for lab environments, emulation environments, or developments where front panel ports are desired.

New Wave DV also offers an optional breakout-panel that cables all 30 ports from the board's high-density connector to a 19-inch rack-mounted 1U panel populated with industry standard 1394b connectors for ease of access and connector strain relief.

Custom Cable
Lengths Available

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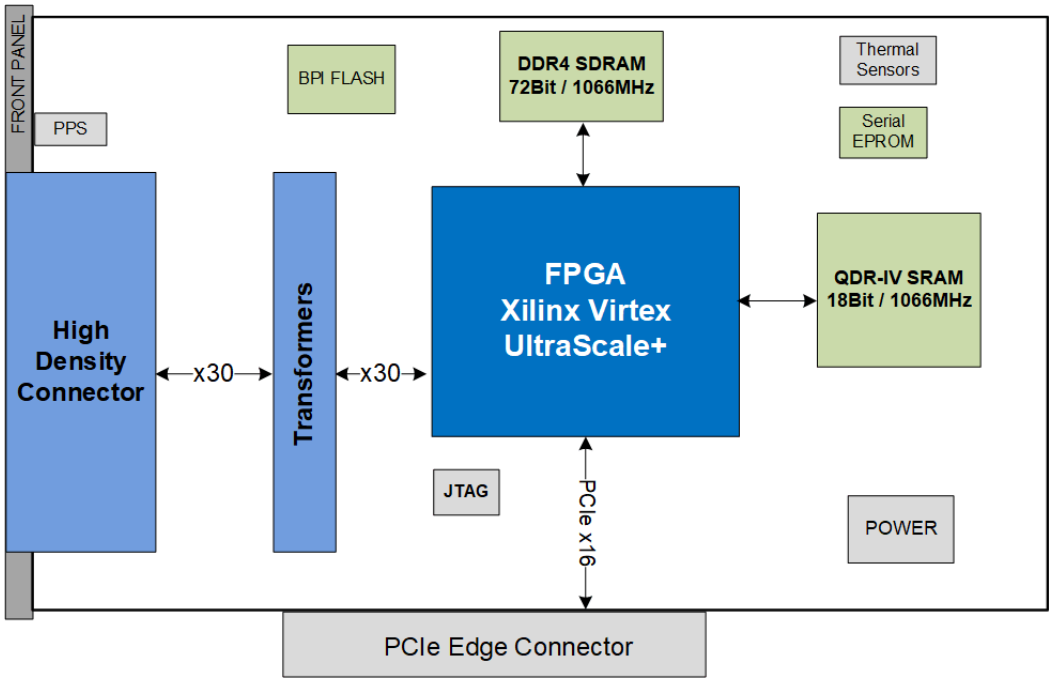

> V5054 Block Diagram

Simplified Programmability Framework

The V5054 can optionally ship with a Development Framework, a fully-integrated and flexible toolset that provides the infrastructure necessary to ensure rapid deployment of custom applications. The framework abstracts the details of the protocol and interfaces, memory controllers and host fabric interfaces, thereby reducing the development effort and schedule for designers to implement custom solutions.

Operation Customization

The V5054 is an FPGA-based network card that can be customized to fit your requirements. New Wave provides access to the FPGA for customers to customize, however New Wave can also modify existing cores or develop new cores for your applications. If you have specific networking requirements, New Wave can help you accomplish your goals.

New Wave DV Mil1394 Enhancements

New Wave DV not only provides IP cores that support industry standard IEEE-1394 OHCI and General Purpose Link Layer Controller (GP2Lynx) along with our proven 1394b PHY IP core. New Wave DV also provides IP Cores specifically optimized for AS5643 (Mil1394) applications. Vehicle system networks (flight controls) require deterministic behavior to ensure timely dissemination, processing and response of all information to ensure safety of flight and vehicle performance requirements.

New Wave DV's OHCI Link Layer IP Core with Start of Frame (STOF) offload engine is designed to move AS5643's strict transmit offset timing requirement from software to hardware. This is accomplished by starting a hardware-based offset timer when a STOF is received and transmitting an Anonymous Subscriber Message (ASM) when the programmed offset time is reached.

The AS5643 Offload Engine IP Core also moves AS5643's strict timing requirements through hardware-based STOF message timing, in addition to providing ASM offload, to ensure multiple transmitted messages are sent at the correct offset times. For receive, the AS5643 Offload Engine provides ASM packet Message-ID-based filtering designed to efficiently place each message directly into host designated memory location.

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Complete Product Support Program

Our customers can attest to our exceptional support. New Wave DV provides an industry-standard warranty on its products, but it is the human factor that makes our support so valuable to our customers. Our team takes the time and effort to ensure a positive customer experience.

Our Commitment

New Wave DV is committed to providing the latest innovations in technology, architectures, and techniques to keep our customers one step ahead of the rest. Our products, complete with the Development Framework, are intended to offer our customers an entirely unique out-of-the-box experience.

Optional Accessories

The V5054 comes standalone or optionally with a 1U 19-inch rack-mount 30-Port 1394b breakout panel accessory. Standard 32" cable included, with custom cable lengths available.

490-05054-02: 1U 19-inch rack-mount 30-Port 1394b breakout panel accessory, with 32" inch cable included

Ordering Information

400-05054-00 (Base Board Configuration): V5054 1394b PCIe FPGA card, 30 front panel transformer-coupled 1394b ports, Xilinx UltraScale KU115 FPGA, 18GB 72-bit DDR4 SDRAM, 144Mbit QDRII+ SRAM, 30 AS5643 Transformer Isolated Ports

Technical Specifications

INTERFACE
Thirty transformer-coupled 1394b ports on front panel

FPGA DEVICE
Xilinx Kintex UltraScale (KU115)

MEMORY
One bank of 4GB to 18GB 72-bit up to 1066MHz DDR4 SDRAM
One bank of 36Mbit to 144Mbit 18-bit 1066MHz QDR-IV SRAM

FLASH
One 32MB memory for storing a default configuration image

HOST INTERFACE
PCI Express Gen3 x 8

EXTERNAL INTERFACE
32 differential pairs (user-configurable)
PPS Interface for time synchronization with µsecond resolution
RS-232 serial interface for debug

THERMAL SENSORS
2 digital temperature sensors

COMPLIANCE
PCI Express Card Electromechanical Specification, Rev 2.0 IEEE FCC 47 CFR Part 15, Subpart B, Class A (USA) IEC 60950-1 (International)
RoHS Directive 2002/95EC

DIMENSIONS
111.15 mm height
254 mm length (card)[1]

POWER REQUIREMENTS
Maximum 65W (preliminary)

TEMPERATURE
Operating: 0 to 45°C
Storage: -40˚C to 85˚C

V5054 Hardware Part Number Configuration

400	-	05054	-	00	-	W
Series		Model		Board Configuration		IP Configuration (Optional)

Select 1 Board Config

400-05054-00-W__

W

Config #		Configuration Option Details				
OHCI w/ STOF Offload	AS5643 Offload	# of Nodes	# of Ports/Node	PHY Core	Default Speed	Linux Driver
01	11	10	3	Y	S200	Y
02	12	10	3	Y	S400	Y
#03 - #10 Reserved	13	15	2	Y	S200	Y
	14	15	2	Y	S400	Y

[1] Power connector is optional, for designs that exceed backplane specific PCIe power specifications. A typical straight mating connector will add an additional 10 mm, and bend radius will add an additional 38 mm for total length of 254 mm + 10 mm + 38 mm = 302 mm. Right angle mating connectors are also available. A typical right angle connector would add 5 mm for a total length of 254 mm + 5 mm = 259 mm.

FOR MORE INFORMATION
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